Acknowledgements

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- One slide was kindly lent to me by Professor Geoff Hall of Imperial College.
- Some come from collaboration WWW sites
Resources (Books)

- Pixel Detectors, Rossi, Fisher, Rohe & Wermes, 2006
- Semiconductor Detector Systems, Spieler, 2005
- Semiconductor Radiation Detectors, Lutz, 1999

Resources (Conferences)

See the proceedings (recent ones on Indico) of the Vertex 20XX and the Pixel 20XX conferences for example.

Vertex 2016: https://indico.cern.ch/event/452781/overview
Pixel 2016: https://agenda.infn.it/conferenceDisplay.py?ovw=True&confId=10190
What is a silicon detector?

- It is a member of a large family of ionisation detectors.
- Related to the gaseous or liquid argon detectors but based on a solid material.
- Nearly all silicon detectors are based on a junction diode. The diodes are reversed biased until fully depleted.
- A MIP particle passing through silicon creates about 8000 electron/hole pairs per 0.1mm. A typical detector element is about 0.3 mm thick.
Basic types

• Silicon strips
  – Implanted p on n gives a single sided detector
  – Adding an n+ implant on the other side makes a double sided detector
  – Typical strips have a pitch of order 0.1 mm

• Pads
  – On single sided detectors. Pads are typically 0.1×0.1 mm²

• Pixels
  – Smaller than pads. The CCD is a special (and important) example of a pixel detector e.g. SLD vertex detector at SLAC.

Dr P R Hobson, Brunel
Silicon diodes as position detectors

- Spatial measurement precision defined by strip dimensions
  - ultimately limited by charge diffusion
  $\sigma \sim 5-10\,\mu m$

Prof G Hall, ICST&M
Examples

• In 1983 NA11 pioneered the use of silicon for track reconstruction in a fixed target experiment to measure charmed particle lifetimes. A readout pitch of 60µm (3 times the actual pitch) was used and a spatial resolution of 5 µm achieved.

• At this time CCD detectors were also being developed for tracking detectors
Examples - LEP

• “Complete” $4\pi$ coverage of silicon detectors for tracking at colliders was a feature of LEP experiments in the 1990’s.
• Major challenge is to package the readout electronics
• ALEPH was first to use double sided vertex detector.
  – Two cylinders with a total of 27 faces each with 4 detectors of 50x50 mm$^2$.
  – Readout at 50 µm in $r$-$\phi$ and 100 µm in $z$.
  – *Multiple scattering* reduced the intrinsic resolution of 12 µm and 17 µm to 20 µm and 40 µm.
• All 4 LEP experiments upgraded to silicon vertex detectors during their operational lifetime.
Aleph

- The silicon vertex detector, 1995 version
H1 at DESY
HERA B

HERA-B Vertex Detector Module

front plane

back plane

double-sided silicon strip detector

ALN carrier

micro adaptor

Al₂O₃

bond joints

electronic hybrids

caption cable

HERA B figures

Diode characteristic
SLD

CCD - VXD3 at SLAC

- Very thin, 0.4% radiation length
- High resolution
  - pixels - 20 µm cubes
  - surface resolution < 4 µm
  - projected impact parameter resolution 11 µm
- Close to beam, inner layer at 2.8 cm radius
- 307 million pixels, < 1 cent/pixel

bb event from SLD WWW site

Figure from talk by H Wieman at Vertex 2000
Double-sided strip

Principle of the double-sided strip detector.

Picture from MPI-HLL (2007)
Resolution

Spatial resolution: strip pitch with interpolation by diffusion (~10 \mu m)

Measured distribution of holes at p\textsuperscript{+} strips

Achieved resolution: ~ 1 \mu m (detector with 20 \mu m pitch NIM235(1985)210)

\[ \Gamma = 8.5 \mu m \quad \text{(measured)} \]
\[ \sigma = 3.0 \mu m \quad \text{precision of single counter} \]

From a lecture by Robert Klanner, Univ. Hamburg
The Inner Tracking System of the ALICE experiment at LHC uses Silicon Drift Detectors in two cylindrical layers located at radial distance of ≈ 15 and ≈ 24 cm from the beam axis.

SDD for ALICE
Silicon Drift - examples

- first realisation (NIM235(1985)231)

example of a vertex detector based on Si-drift chambers (STAR detector at RHIC, BNL - NIMA 541(2005)57)

- position resolution vs drift field →
  ~ 5µm achieved
  Laser spot

- excellent 2d position resolution with small no. of read-out channels but
- speed (several 100 ns drift times)
- sensitivity to radiation

drift principle → many applications!

From a lecture by Robert Klanner, Univ. Hamburg
Evolution of scale

Moore’s Law for Silicon Detectors

<table>
<thead>
<tr>
<th>Year</th>
<th>2005</th>
<th>2010</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si Area [m²]</td>
<td>230 (CMS)</td>
<td>2,000</td>
</tr>
<tr>
<td># of Channels</td>
<td>10M (CMS)</td>
<td>100M</td>
</tr>
<tr>
<td>Cost [$/cm²]</td>
<td>5 (CMS)</td>
<td>&lt; 2</td>
</tr>
</tbody>
</table>

Silicon Area [m²]

[# of Electronics Channels [in k]]
Design Drivers: Resources and Speed

Growth with time

- Limited Resources (Power)
- Long Ladders, slow

"Short" strips, Fast
But power/cooling is not free!

Long Ladders possible with:
Bonding and Encapsulation
“Hybrid” Pixels

Summary Hybrid Pixel Detectors

- technology well developed, m^2s used in LHC-experiments (ALICE, ATLAS, CMS), synchrotron rad., radiology,…
- already experience in actual experiments
- high degree of flexibility in design \(\rightarrow\) many developments in progress!
- radiation hardness achieved,
- “any” detector material possible (Si, GaAs, CdTe,…)
- typical pixel dimensions > 50 \(\mu m\),
- high speed: e.g. 1 MHz/pixel,
- (effective) noise \(\sim100e\) achieved
- limitations for particle physics is detector thickness, power and possibly minimum pixel size

From a lecture by Robert Klanner, Univ. Hamburg
"Monolithic" Pixels

8.7 Monolithic Pixel Detectors

**Idea**: radiation detector + amplifying + logic circuitry on single Si-wafer
- dream! 1st realisation already in 1992
- strong push from ILC → minimum thickness, size of pixels and power!
- so far no large scale application in research (yet)

**CMOS Active Pixels**
(used in commercial CMOS cameras)

**Principle**: 

- technology in development - with many interesting results already achieved
  
  **example**: MIMOSA (built by IReS-Strasbourg; tests at DESY + UNIHH)
  
  - 3.5 cm² produced by AMS (0.6 μm)
  - 14 μm epi-layer, (17 μm)² pixels
  - 4 matrices of 512² pixels
  - 10 MHz read-out (→ 50 μs)
  - 120 μm thick

From a lecture by Robert Klanner, Univ. Hamburg
PHYSICS REQUIREMENTS at the LHC and SLHC ($10^{35}\text{cm}^2\text{s}^{-1}$)

Most probable Higgs channel

REQUIRED PRECISE MEASUREMENTS OF

- MOMENTUM RESOLUTION
- TRACK RECONSTRUCTION
- b-TAGGING EFFICIENCY

REQUIRED PRECISE MEASUREMENTS OF

- ACCURACY OF STANDARD MODEL PARAMETERS
- ACCURACY OF NEW PHYSICS PARAMETERS
- SUPERSYMMETRIC PARTICLES
- EXTRA DIMENSIONS
- RARE PROCESSES (TOP DECAYS, HIGGS PAIRS ETC)

GOOD TRACKER ESSENTIAL!
Radiation Induced Bulk Damage in Silicon

Van Lint 1980

Primary Knock on Atom

Displacement threshold in Si:
Frenkel pair $E \approx 25\text{eV}$
Defect cluster $E \approx 5\text{keV}$

Vacancy

Interstitial
Radiation Induced Defects in Silicon

**Neutron irradiated** From RD48/rose

DLTS spectrum

- **V₁, I** migrate until they meet impurities and dopants to form stable defects
- Charged defects \( \Rightarrow N_{\text{eff}}, V_{\text{bias}} \)
- Deep traps, recombination centers \( \Rightarrow \text{charge loss} \)
- Generation centers \( \Rightarrow \text{leakage current} \)

\[
\begin{align*}
E_c & \quad \text{V}_6 \\
& \quad \text{VO}^- \quad E_c - 0.17 \text{eV} \\
& \quad \text{V}_2(=\sim)+V_n \quad E_c - 0.22 \text{eV} \\
& \quad \text{V}_2(-\sim)+V_n \quad E_c - 0.40 \text{eV} \\
E_i & \quad \text{V}_2O \\
E_v & \quad \text{C}_1\text{O}_1^{(0/+)} \quad E_v + 0.36 \text{eV} \\
\end{align*}
\]

\( \text{VO} \) effective e and h trap

\( \text{V}_2 \) and \( \text{V}_2O \) deep acceptors contribute to \( N_{\text{eff}} \)

Dr C Da Via, Brunel
MAIN DETECTOR STRATEGIES AVAILABLE FOR LIFE ABOVE $10^{15}$ n/cm$^2$

OPTIMIZATION OF:
- COLLECTION DISTANCE
- CCE (trapping)
- SPEED
- SPACE CHARGE
- REVERSE ANNEALING
- CCE (underdepletion)
- CHARGE SHARING
- LEAKAGE CURRENT

MORE TO GAIN BY COMBINING TECHNIQUES!

BY IMPROVING:
- DEVICE GEOMETRY
  - 3D, THIN
- DETECTOR BULK
  - O, O$_2$ P-TYPE
- MODE OF OPERATION
  - Temperature, Forward bias

Dr C Da Via, Brunel
SHORT DRIFT LENGTH USING 3D DETECTORS

S. Parker, C. Kenney
1995

- FZ silicon
- p-type substrate
- High resistivity $k\Omega \cdot cm$
- $<100>$ orientation

3D VERSUS PLANAR

- COLLECTION PATHS
- DEPLETION VOLTAGES
- CHARGE COLLECTION
- EDGE SENSITIVITY
- AREA COVERAGE

3D
- Collection paths: ~50 µm
- Depletion voltages: < 10 V
- Charge collection: 1-2 ns
- Edge sensitivity: < 10 µm
- Area coverage: active edges

Planar
- Collection paths: 300 µm
- Depletion voltages: 70 V
- Charge collection: 10-20 ns
- Edge sensitivity: 300 µm
- Area coverage: other

Dr C Da Via, Brunel
3D DETECTOR RESULTS before irradiation

DETECTOR THICKNESS 121µm
282e noise PREAMP - SHAPING TIME 1 µs
200 µm PITCH µSTRIP TYPE DETECTOR

GAUSSIAN RESPONSE

SPEED
1.5ns rise AT 130K
3.5ns rise AT 300K

350 e rms, fast electronic designed at CERN-microelectronics group
200µm pitch detector, Berunel, Cern, Hawaii, TO BE PUBLISHED
Upgrades are in progress or planned for the LHC experiments

**Outer Trackers – Strips and strixels**
- Bulk material type: p-type for higher signal and robust, cost effective process
- Choice of FZ/MCz, thickness and oxygen concentration
- Optimize strip geometry, length, isolation
- Large scale production of cheap, thinned modules

**Inner Trackers - Pixels**
- Predominantly p-type
- Layers 2 - 4: $5 \times 10^{15} - 1.5 \times 10^{15} n_{eq}$
- Layer 1: up to $2 \times 10^{16}$: planar/3D/Diamond?
- Explore process limits for fine pitch sensors
- Sparking, Interconnection issue
- Large scale production of cheap, thinned modules
Current planar pixel detectors rad hard to $\sim 10^{15}$
What are the HL-LHC baseline solutions?
What are the challenges?

- Decreasing inactive edges
- Sparking at sensor edge
- Modified Pixel geometries
- Smaller pitches
- ROC tiling on large sensor
- Sensor bulk material choice
- Sensor/ASIC thickness
- Move to 3d technology

Paula Collins
ECFA High Luminosity LHC Experiments Workshop

10/21/14
Future trend example

Integrate readout with the silicon sensor

- Advantages in integration, cost, potentially strong impact on power consumptive and material budget
- in two experiments: DEPFET in Belle-II and MAPS in STAR
- not yet in LHC, adopted for ALICE ITS upgrade, considered for CLIC/ILC

Traditional Monolithic Active Pixel Sensors (MAPS)

- Commercial CMOS technologies
- No reverse substrate bias:
  - Signal charge collection mainly by diffusion
  - sensitive to displacement damage
- Only one type of transistor in pixel (twin well)
  - Very simple in-pixel circuit (few transistors)
  - pixel size: 20 x 20 μm² or lower
- Rolling shutter readout: serial, row-by-row, not very fast

Main challenge for improvement: need combination of:
- tolerance to displacement damage (depletion)
- integration of complex circuitry without efficiency loss
- keep using commercial technology

From talk at ECFA 2014 meeting by W Snoeys
- Producing particle sensors in CMOS technologies would provide cost savings, progress is being made, but combining low power and radiation tolerance sufficient for HL-LHC in a commercial CMOS technology is still a challenge.

- CMOS MAPS: integrate the full readout into the sensor
  - advantages in terms of assembly, production cost and Q/C
  - adopted for the ALICE ITS upgrade:
    - full-scale prototypes meet specifications
    - sensor optimization (Q/C) for low analog power
    - soldering pads over matrix, thinning, soldering.

- HV/HR CMOS: analog active sensor and modified digital readout chip
  - ATLAS HV/HR CMOS collaboration:
  - promising results for aggressive environments, still challenges: will investigate higher resistivity substrates in HV technologies and imaging technologies
goal: large size demonstrator by the end of 2015.