Evolution of the Digital Circuits with Variable Layouts

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Abstract

We use evolutionary search to design combinational logic circuits which is based on evolving the functionality and connectivity of a rectangular array of logic cells in addition to the layout of this array. The evolutionary process contains two main steps. Initially the genome fitness in given by the percentage of output bits, which are correct. Once 100% functional circuits have been evolved, the number of gates actually used in the circuit is taken into account in the fitness function. This allows us to evolve circuit with 100% functionality *and* minimise the number of active gates in circuit structure.

1 PROBLEM DESCRIPTION

The choice of suitable circuit layout is very complicated task and is intimately linked the complexity of function implemented (Kalganova, 1998). So, we have tried to solve this problem by evolving the circuit layout at the same time as trying to evolve 100% functional circuits.

There are two aspects required to define any combinational logic network. The first is the cell-level functionality and the second is the inter-connectivity of the cells between the circuit inputs and outputs. An encoding of the chromosome was adopted that satisfies these two aspects.

A combinational circuit is represented as a rectangular array of logic gates. Each logic cell in this array is uncommitted and can be removed from the network if they prove to be redundant. The inputs of the combinational network such as logical constants, primary and inverted inputs, as well as the outputs of logic cells are labelled with an individual integer. We define each logic function to be chosen from the set of functions AND, OR, NOT, EXOR and multiplexer with primary and inverted inputs. Each input of a logic gate may be connected to the output of a logic gate provided it is to the left of the cell, a logical constant, a primary input or an inverted primary input.

The chromosome is represented by a 3-level structure: 1) Layout structure; 2) Circuit structure; 3) Gate (cell) structure. On the first level the global characteristics of the circuit are defined. There are levels-back parameter and the number of rows and columns. On the second level the array of cells are created and the circuit outputs are determined. Finally the third level represents the structure of each cell in the circuit. The data describing the cell contains the number of inputs, the array of inputs and the functional gene. The number of inputs in the cell depends on the type of cell and is defined when the value of functional gene is known.

2 CONCLUSION

In the series of experiments the proportion of gates used in the circuit is investigated as a function of the maximum number of gates available. It was found that the proportion of active and unused gates is constant with increasing the number of gates in circuit structure. This means that the number of active gates grows in linear way with increasing the number of possible gates in circuit. It implies that the most economical circuit will not occur often in larger circuits. The proportion varies erratically with smaller number of gates.

A study of many histories of the GA runs revealed that the evolution proceeds in the three successive phases:
1. in the early generations, the population selects a particular circuit layout;
2. in the second phase, the structure of the circuit evolves in such a way, that the circuit implements the test function;
3. in the last phase, the evolution process is slower and tends to decrease the number of gates in the actual circuit.

Thus we can argue that since the circuit layout is chosen so early in the history of the GA evolution is proceeding with a largely fixed geometry.

References

Kalganova, T., J. Miller and T. Fogarty (1998). Some Aspects of an Evolvable Hardware Approach for Multiple-Valued Combinational Circuit Design in *Proc. Of the 2nd Int. Conf. on Evolvable Systems (ICES'98).* Lausanne, Switzerland, Edited by M. Sipper, D. Mange, A. Perez-Uribe. Springer-Verlag, pp. 78-89, 1998.